OKAYA Electric America, Inc.

SPECIFICATIONS

DRAWING CODE _____

SAMPLE CODE _____

(This Code will be changed while mass production)

MASS PRODUCTION CODE **RW12864E-L3N-OT**

Customer Approved

Date:

Sales Sign	QC Confirmed	Checked By	Designer

Approval for Specifications Only

This specification is subject to change without notice

Approval for Specifications and Sample

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MODLE NO：

RECORDS OF REVISION			DOC. FIRST ISSUE
VERSION	DATE	REVISED PAGE NO.	**SUMMARY**
0	2013.01.15		First issue
A	2013.01.17	6	Correct Active Area

2. General Description

Item	Dimension	Unit
Number of Characters	128 x 64 Dots	-
Module dimension	75.0 × 52.7 × 8.5 (mm)	mm
Active Area	53.73 × 26.85 (mm)	mm
Pixel Pitch	0.42 × 0.42 (mm)	mm
Pixel Size	0.39 × 0.39 (mm)	mm
Weight	24.5	g
Display Mode	Passive Matrix	
Display Color	Monochrome (Yellow)	
Drive Duty	1/64 Duty	

3. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	VDD	-0.3	3.5	V	1,2
Supply Voltage for Display	VCC	8	16	V	1,2
Operating Temperature	TOP	-40	80	℃	—
Storage Temperature	TSTG	-40	80	℃	—

Note 1: All the above voltages are on the basis of “VSS = 0V”.

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3.“Optics & Electrical Characteristics”. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

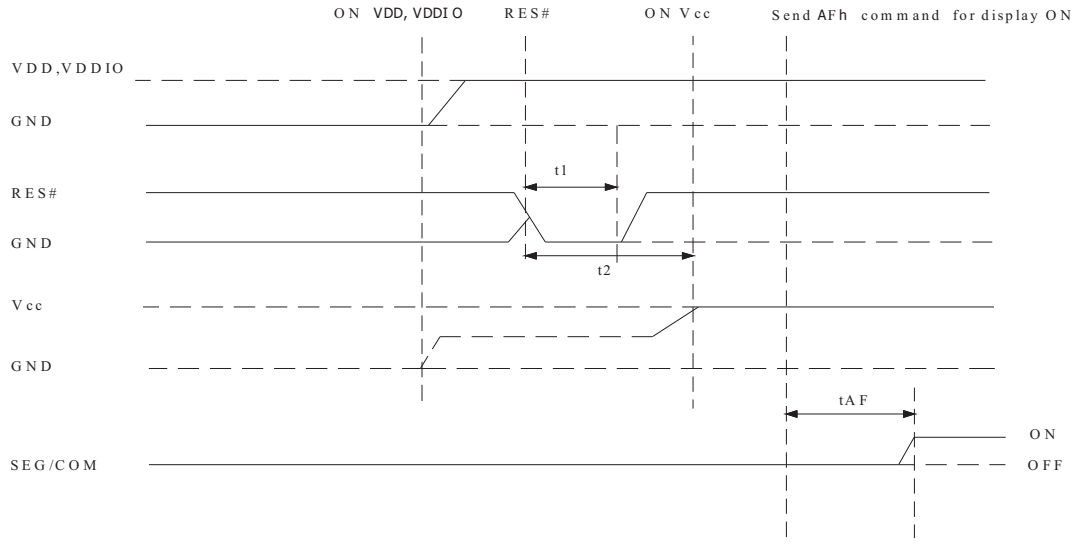
4. Block Diagram

4.1.POWER ON/OFF SEQUENCE &APPLICATION CIRCUIT

3.1.1 POWER ON/OFF SEQUENCE

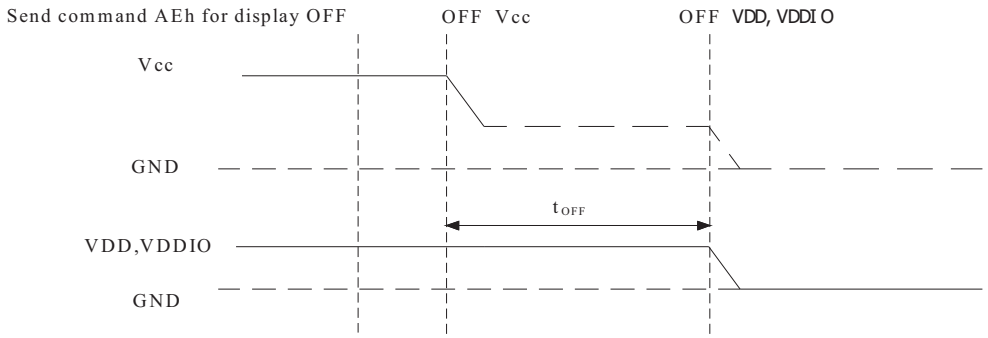
Power ON sequence

1. Power ON VDD ,VDDIO
2. After VDD ,VDDIO become stable , set RES# pin LOW (logic low) for at least 3us(t1) and then HIGH (logic high).
3. After set RES# pin LOW (logic low),wait for at least 3us(t2). Then Power ON Vcc. (1)
4. After Vcc. become stable , send command AFh for display ON. DEG/COM will be ON after 100ms(tAF).



Power OFF sequence

1. Send command AEh for display OFF.
2. Power OFF Vcc.(1),(2)
3. Wait for tOFF. Power OFF VDD ,VDDIO. (where Minimum tOFF=80ms,Typical tOFF=100ms)



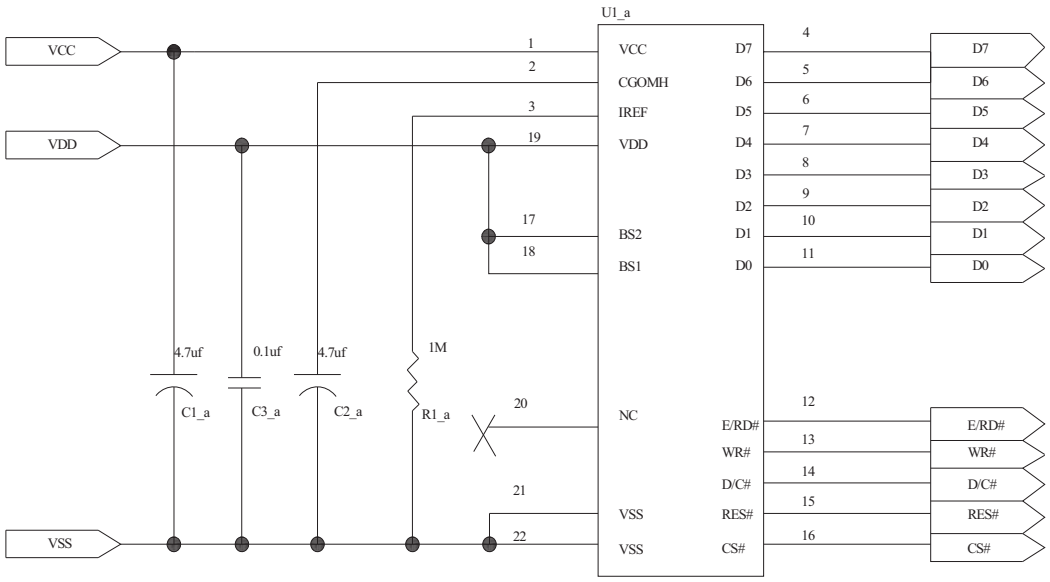
Note:

(1) Since an ESD protection circuit is connected between VDD ,VDDIO and Vcc, Vcc

becomes lower than VDD and VDD , VDDIO is ON and Vcc is OFF as shown in the dotted line of Vcc in above figures.

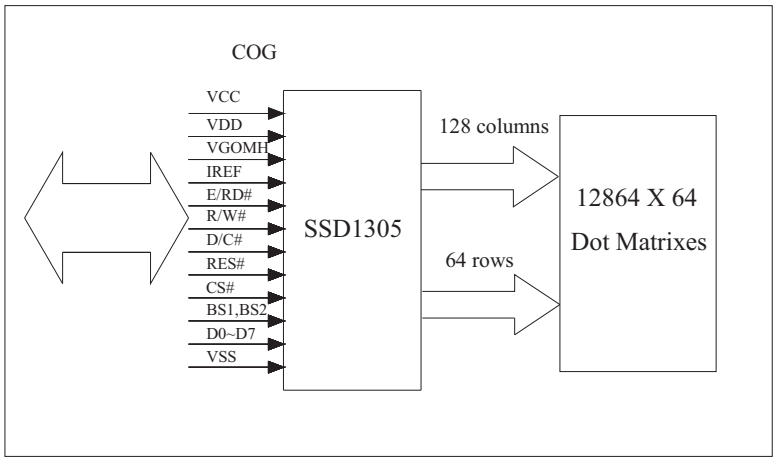
(2) Vcc should be disabled when it is OFF.

4.2 APPLICATION CIRCUIT

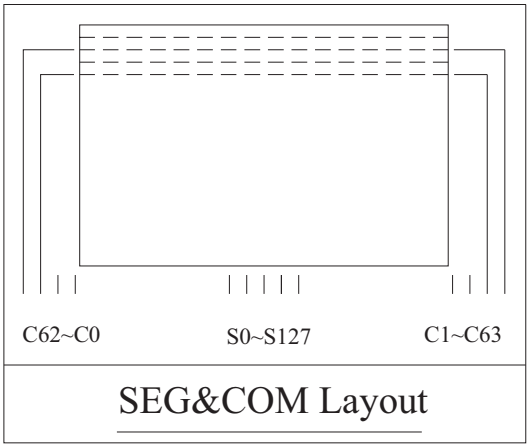


4.3 INTERFACE

4.3.1 FUNCTION BLOCK DIAGRAM



4.4 PANEL LAYOUT DIAGRAM



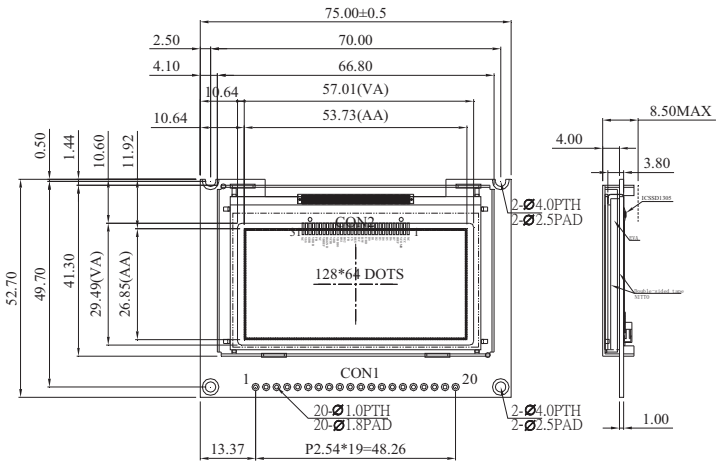
4.5 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 132x64=8448bits

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

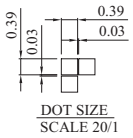
					SEG0	SEG0	SEG0	SEG0	SEG0	SEG0	SEG0	SEG0		SEG0	SEG0	SEG0	SEG0
					0x83h	0x82h	0x81h	0x80h	0x7Fh	0x7Eh	0x7Dh	0x7Ch		0x03h	0x02h	0x01h	0x00h
					0x00h	0x01h	0x02h	0x03h	0x04h	0x05h	0x06h	0x07h		0x80h	0x81h	0x82h	0x83h
COM0	0x3Fh	0x00h	PAGE 0	D0													
COM1	0x3Eh	0x01h		D1													
COM2	0x3Dh	0x02h		D2													
COM3	0x3Ch	0x03h		D3													
COM4	0x3Bh	0x04h		D4													
COM5	0x3Ah	0x05h		D5													
COM6	0x39h	0x06h		D6													
COM7	0x38h	0x07h		D7													
COM8	0x37h	0x08h	PAGE 1	D0			■	■	■	■							
COM9	0x36h	0x09h		D1		■					■						
COM10	0x35h	0x0Ah		D2		■					■						
COM11	0x34h	0x0Bh		D3		■					■						
COM12	0x33h	0x0Ch		D4		■					■						
COM13	0x32h	0x0Dh		D5		■					■						
COM14	0x31h	0x0Eh		D6		■					■						
COM15	0x30h	0x0Fh		D7			■	■	■	■							
COM16	0x2Fh	0x10h	PAGE 2	D0													
COM17	0x2Eh	0x11h		D1													
COM18	0x2Dh	0x12h		D2													
COM19	0x2Ch	0x13h		D3													
COM20	0x2Bh	0x14h		D4													
COM21	0x2Ah	0x15h		D5													
COM22	0x29h	0x16h		D6													
COM23	0x28h	0x17h		D7													
COM48	0x0Fh	0x30h	PAGE 6	D0													
COM49	0x0Eh	0x31h		D1													
COM50	0x0Dh	0x32h		D2													
COM51	0x0Ch	0x33h		D3													
COM52	0x0Bh	0x34h		D4													
COM53	0x0Ah	0x35h		D5													
COM54	0x09h	0x36h		D6													
COM55	0x08h	0x37h		D7													
COM56	0x07h	0x38h	PAGE 7	D0													
COM57	0x06h	0x39h		D1													
COM58	0x05h	0x3Ah		D2													
COM59	0x04h	0x3Bh		D3													
COM60	0x03h	0x3Ch		D4													
COM61	0x02h	0x3Dh		D5													
COM62	0x01h	0x3Eh		D6													
COM63	0x00h	0x3Fh		D7													

5. Contour Drawing



CON1	
PIN NO.	SYMBOL
1	VDD
2	VSS
3	NC
4	DB0
5	DB1
6	DB2
7	DB3
8	DB4
9	DB5
10	DB6
11	DB7
12	CS
13	NC
14	/RES
15	R/W
16	D/C
17	E
18	NC
19	DISP
20	NC

The non-specified tolerance of dimension is ±0.3mm.



DOT SIZE
SCALE 20/1

6. Interface Pin Function

No.	Symbol	Function
1	VDD	Power supply for analog circuit.
2	VSS	Ground.
3	NC	No connection
4~11	D0~D7	Data bus.
12	CS#	Chip select input.
13	NC	No connection
14	RES	Reset signal input. When it's low, initialization of SSD1305 is executed.
15	R/W	Data write operation is initiated when it's pull low.
16	D/C	Data/ Command control. Pull high for write/read display data. Pull low for write command or read status.
17	E	Data read operation is initiated when it's pull low.
18	NC	No connection
19	DISP	Display off
20	NC	No connection

8080 INTERFACE.

7. Optics & Electrical Characteristics

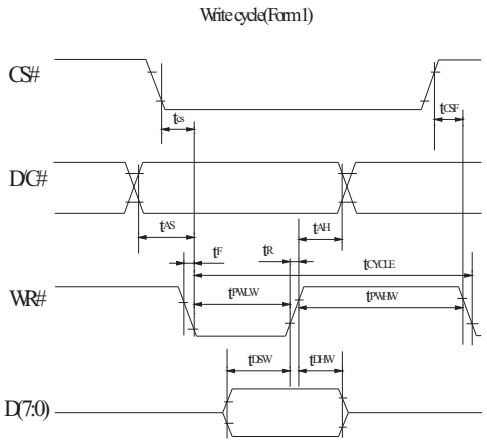
7.1INTERFACE TIMING CHART

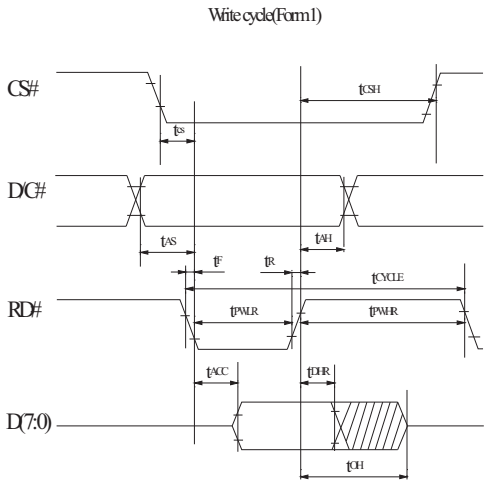
8080-Series MCU Parallel Interface Timing Characteristics

(VDD-VSS=2.4V to 3.5V, VDDIO=VDD,TA=25℃)

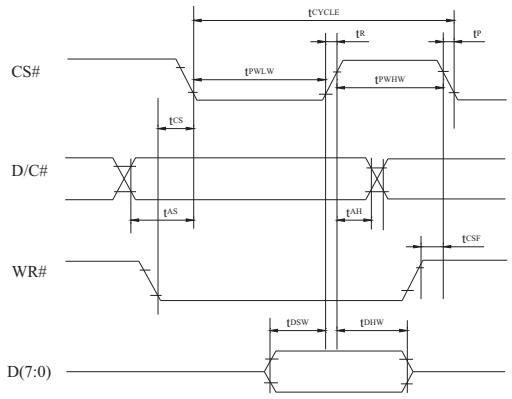
Symbol	Parameter	Min	Typ	Max	Unit
tcycle	Clock Cycle Time	300	-	-	ns
tAS	Address Setup Time	10	-	-	ns
tAH	Address Hold Time	0	-	-	ns
tDSW	Write Data Setup Time	40	-	-	ns
tDHW	Write Data Hold Time	7	-	-	ns
tDHR	Read Data Hold Time	20	-	-	ns
tOH	Output Disable Time	-	-	70	ns
tACC	Access Time	-	-	140	ns
tPWLR	Read Low Time	120	-	-	ns
tPWLW	Write Low Time	60	-	-	ns
tPWHR	Read High Time	60	-	-	ns
tPWHW	Write High Time	60	-	-	ns
tR	Rise Time	-	-	15	ns
tF	Fall Time	-	-	15	ns
tCS	Chip select setup time	0	-	-	ns
tCSH	Chip select setup hold time to read signal	0	-	-	ns
tCSF	Chip select setup hold time	20	-	-	ns

8080-seriesparallel interface characteristics (Form 1)

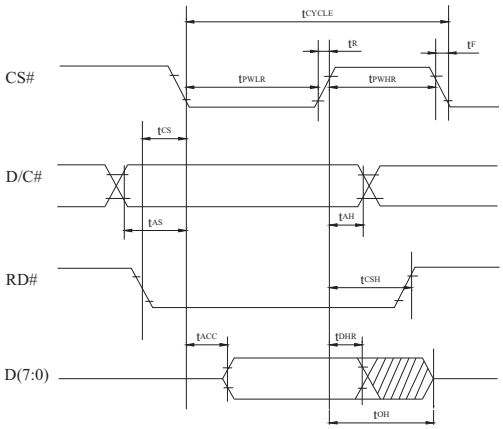




Write cycle(Form 2)



Write cycle(Form 2)



7.2 DC Characteristics

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage for Logic	VDD	—	2.4	2.7	3.5	V
Supply Voltage for Display	VCC	—	11.0	13.0	15.0	V
High Level Input	VIH	Iout = 100μA,3.3MHz	0.8×VDD	—	VDD	V
Low Level Input	VIL	Iout = 100μA,3.3MHz	0	—	0.2×VDD	V
High Level Output	VOH	Iout =100μA,3.3MHZ	0.9×VDD	—	VDD	V
Low Level Input	VOL	Iout =100μA,3.3MHZ	0	—	0.1×VDD	V
Operating Current for VDD	IDD	Note 4	—	45	—	mA
Sleep Mode Current for VDD	IDD, SLEEP		—	—	1.5	mA

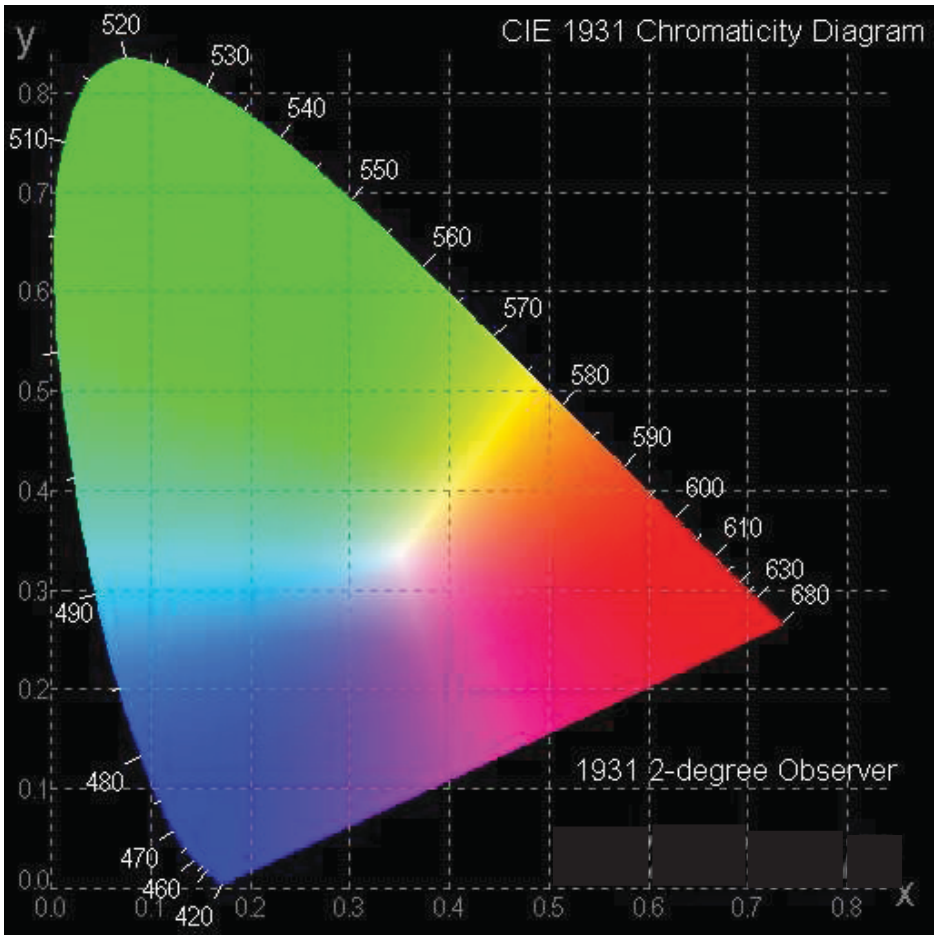
Note 3: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.

Note 4: V_{DD} = 2.7V, V_{CC} = 13V, 50% Display Area Turn on.

* Software configuration follows Section 4.4 Initialization.

7.3 Optics Characteristics

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
C.I.E. (Yellow)	(x) (y)	Without Polarizer	0.43 0.46	0.47 0.50	0.51 0.54	
Dark Room Contrast	CR		—	>2000:1	—	—
View Angle			>160	—	—	
Brightness	Yellow	With Polarizer	60	80	—	cd/m^2



8. Reliability

8.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation Low Temperature Operation	80℃,240hrs -40℃,240hrs	The operational functions work.
High Temperature Storage Low Temperature Storage	80℃,240hrs -40℃,240hrs	
High Temperature/Humidity Operation/ Thermal Shock	60℃,90%RH,120hrs，-40℃80℃，24cycles 1 hr dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

8.2 Lifetime

Parameter	Min	Typ	Max	Unit	Condition	Notes
Operating Life Time		100,000	—	Hrs	80 cd/m2, 50% Checkerboard	6

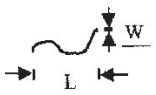
Note 6: The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

8.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5℃; 55±15% RH.

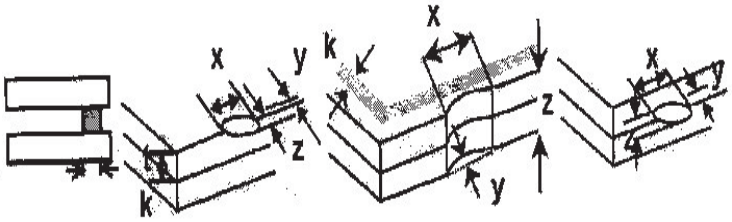
Note.
1.It's pretty common to use "Screen Saver" to extend the lifetime and Don't use fix information for long time in real application.
2.Don't use fixed information in OLED panel for long time, that will extend "screen burn" effect time

9. Inspection specification

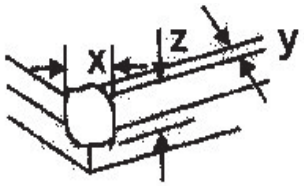
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>01</td><td>Electrical Testing</td><td>1.1 Missing vertical, horizontal segment, segment contrast defect.
1.2 Missing character , dot or icon.
1.3 Display malfunction.
1.4 No function or no display.
1.5 Current consumption exceeds product specifications.
1.6 Viewing angle defect.
1.7 Mixed product types.
1.8 Contrast defect.</td><td>0.65</td></tr>
<tr><td>02</td><td>Black or white spots (display only)</td><td>2.1 White and black spots on display ≦0.25mm, no more than three white or black spots present.
2.2 Densely spaced: No more than two spots or lines within 3mm</td><td>2.5</td></tr>
<tr><td rowspan="2">03</td><td rowspan="2">Black spots, white spots, contamination (non-display)</td><td>3.1 Round type : As following drawing
Φ=(x + y) / 2</td><td>2.5</td></tr>
<tr><td>3.2 Line type : (As following drawing)
 

<table><tr><th>Length</th><th>Width</th><th>Acceptable Q TY</th></tr><tr><td>---</td><td>W≦0.02</td><td>Accept no dense</td></tr><tr><td>L≦3.0</td><td>0.02＜W≦0.03</td><td rowspan="2">2</td></tr><tr><td>L≦2.5</td><td>0.03＜W≦0.05</td></tr><tr><td>---</td><td>0.05＜W</td><td>As round type</td></tr></table></td><td>2.5</td></tr>
<tr><td>04</td><td>Polarizer bubbles</td><td>If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction.
<table><tr><th>Size Φ</th><th>Acceptable Q TY</th></tr><tr><td>Φ≦0.20</td><td>Accept no dense</td></tr><tr><td>0.20＜Φ≦0.50</td><td>3</td></tr><tr><td>0.50＜Φ≦1.00</td><td>2</td></tr><tr><td>1.00＜Φ</td><td>0</td></tr><tr><td>Total Q TY</td><td>3</td></tr></table></td><td>2.5</td></tr>
</table>

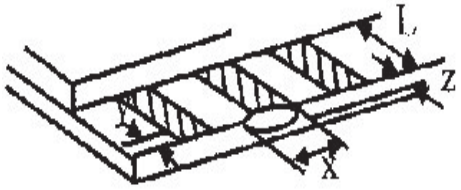
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>05</td><td>Scratches</td><td>Follow NO.3 Black spots, white spots, contamination</td><td></td></tr>
<tr><td>06</td><td>Chipped glass</td><td>Symbols Define:
x: Chip length y: Chip width z: Chip thickness
k: Seal width t: Glass thickness a: Side length
L: Electrode pad length:

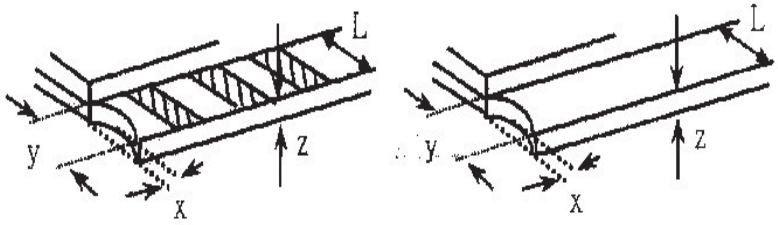
6.1 General glass chip :
6.1.1 Chip on panel surface and crack between panels:
 

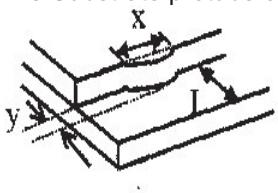
<table><tr><th>z: Chip thickness</th><th>y: Chip width</th><th>x: Chip length</th></tr><tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr><tr><td>1/2t＜z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr></table>⊙If there are 2 or more chips, x is total length of each chip.

6.1.2 Corner crack:
 

<table><tr><th>z: Chip thickness</th><th>y: Chip width</th><th>x: Chip length</th></tr><tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr><tr><td>1/2t＜z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr></table>⊙If there are 2 or more chips, x is the total length of each chip.</td><td>2.5</td></tr>
</table>

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>06</td><td>Glass crack</td><td>
Symbols :
x: Chip length y: Chip width z: Chip thickness
k: Seal width t: Glass thickness a: Side length
L: Electrode pad length
6.2 Protrusion over terminal :
6.2.1 Chip on electrode pad :


<table>
<tr><th>y: Chip width</th><th>x: Chip length</th><th>z: Chip thickness</th></tr>
<tr><td>y≦0.5mm</td><td>x≦1/8a</td><td>0 ＜ z ≦ t</td></tr>
</table>
6.2.2 Non-conductive portion:


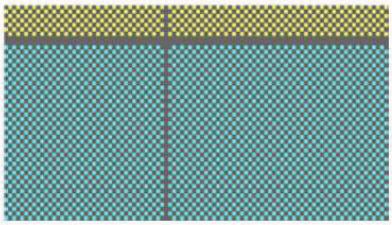
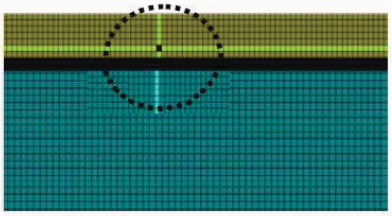
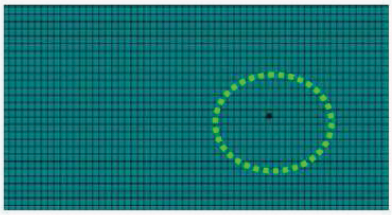
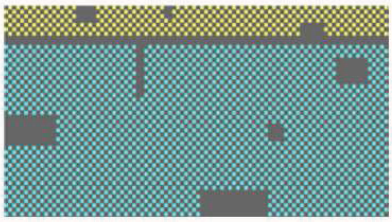
<table>
<tr><th>y: Chip width</th><th>x: Chip length</th><th>z: Chip thickness</th></tr>
<tr><td>y≦ L</td><td>x≦1/8a</td><td>0 ＜ z ≦ t</td></tr>
</table>
⊙If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.
⊙If the product will be heat sealed by the customer, the alignment mark not be damaged.
6.2.3 Substrate protuberance and internal crack.


<table>
<tr><th>y: width</th><th>x: length</th></tr>
<tr><td>y≦1/3L</td><td>x ≦ a</td></tr>
</table>
</td><td>2.5</td></tr>
</table>

NO	Item	Criterion	AQL
07	Cracked glass	With extensive crack is not acceptable.	2.5
08	Backlight elements	8.1 Illumination source flickers when lit. 8.2 Spots or scratched that appear when lit must be judged. Using Spot, lines and contamination standards. 8.3 Backlight doesn't light or color wrong.	0.65 2.5 0.65
09	Bezel	9.1 Bezel may not have rust, be deformed or have fingerprints, stains or other contamination. 9.2 Bezel must comply with job specifications.	2.5 0.65
10	PCB、COB	10.1 COB seal may not have pinholes larger than 0.2mm or contamination. 10.2 COB seal surface may not have pinholes through to the IC. 10.3 The height of the COB should not exceed the height indicated in the assembly diagram. 10.4 There may not be more than 2mm of sealant outside the seal area on the PCB. And there should be no more than three places. 10.5 No oxidation or contamination PCB terminals. 10.6 Parts on PCB must be the same as on the production characteristic chart. There should be no wrong parts, missing parts or excess parts. 10.7 The jumper on the PCB should conform to the product characteristic chart. 10.8 If solder gets on bezel tab pads, LED pad, zebra pad or screw hold pad, make sure it is smoothed down.	2.5 2.5 0.65 2.5 2.5 0.65 0.65 2.5
11	Soldering	11.1 No un-melted solder paste may be present on the PCB. 11.2 No cold solder joints, missing solder connections, oxidation or icicle. 11.3 No residue or solder balls on PCB. 11.4 No short circuits in components on PCB.	2.5 2.5 2.5 0.65

NO	Item	Criterion	AQL
12	General appearance	12.1 No oxidation, contamination, curves or, bends on interface Pin (OLB) of TCP. 12.2 No cracks on interface pin (OLB) of TCP. 12.3 No contamination, solder residue or solder balls on product. 12.4 The IC on the TCP may not be damaged, circuits. 12.5 The uppermost edge of the protective strip on the interface pin must be present or look as if it cause the interface pin to sever. 12.6 The residual rosin or tin oil of soldering (component or chip component) is not burned into brown or black color. 12.7 Sealant on top of the ITO circuit has not hardened. 12.8 Pin type must match type in specification sheet. 12.9 Pin loose or missing pins. 12.10 Product packaging must the same as specified on packaging specification sheet. 12.11 Product dimension and structure must conform to product specification sheet.	2.5 0.65 2.5 2.5 2.5 2.5 2.5 0.65 0.65 0.65 0.65

Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major